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# UTILITY PATENT APPLICATION TRANSMITTAL

*(Only for new nonprovisional applications under 37 C.F.R § 1.53(b))*

| | |
|---|---|
| *Attorney Docket No.* | 367.39268X00 |
| *First Inventor or Application Identifier* | Soren NORSKOV |
| *Title* | See 1 in Addendum |
| *Express Mail Label No.* | |



## APPLICATION ELEMENTS

*See MPEP chapter 600 concerning utility patent application contents.*

*ADDRESS TO:* Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. [X] * Fee Transmittal Form *(e.g., PTO/SB/17)*
*(Submit an original and a duplicate for fee processing)*

2. [X] Specification [Total Pages 12 ]
*(preferred arrangement set forth below)*
- Descriptive title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings *(if filed)*
- Detailed Description
- Claim(s)
- Abstract of the Disclosure

3. [X] Drawing(s) *(35 U.S.C. 113)* [Total Sheets 3 ]

4. Oath or Declaration [Total Pages 2 ]
   a. [X] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 C.F.R. § 1.63(d))
   *(for continuation/divisional with Box 16 completed)*
      i. [ ] DELETION OF INVENTOR(S)
      Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).

** NOTE FOR ITEMS 1 & 13 IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C.F.R. § 1.27), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C.F.R. § 1.28).*

5. [ ] Microfiche Computer Program *(Appendix)*

6. Nucleotide and/or Amino Acid Sequence Submission
*(if applicable, all necessary)*
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

## ACCOMPANYING APPLICATION PARTS

7. [X] Assignment Papers (cover sheet & document(s))
8. [ ] 37 C.F.R.§3.73(b) Statement *(when there is an assignee)* [X] Power of Attorney
9. [ ] English Translation Document *(if applicable)*
10. [X] Information Disclosure Statement (IDS)/PTO-1449 [X] Copies of IDS Citations
11. [X] Preliminary Amendment
12. [X] Return Receipt Postcard (MPEP 503)
*(Should be specifically itemized)*
13. [ ] * Small Entity Statement(s) *(PTO/SB/09-12)* [ ] Statement filed in prior application Status still proper and desired
14. [X] Certified Copy of Priority Document(s)
*(if foreign priority is claimed)*
15. [X] Other: See 2 in Addendum

16. **If a CONTINUING APPLICATION,** *check appropriate box, and supply the requisite information below and in a preliminary amendment:*
[ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No. _____/_____
*Prior application information:* Examiner _____ *Group / Art Unit.* _____

**For CONTINUATION or DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.**

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|---|---|---|---|
| *Name (Print/Type)* | Carl J. Brundidge | *Registration No. (Attorney/Agent)* | 29,621 |
| *Signature* | | *Date* | 11-27-00 |

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# FEE TRANSMITTAL for FY 2000

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*See 37 C.F.R. §§ 1.27 and 1.28.*

**TOTAL AMOUNT OF PAYMENT** ($) 990.00

| Complete if Known | |
|---|---|
| Application Number | |
| Filing Date | November 27, 2000 |
| First Named Inventor | Soren NORSKOV |
| Examiner Name | |
| Group / Art Unit | |
| Attorney Docket No. | 367.39268X00 |

jc918 U.S. PTO 09/721677 11/27/00

## METHOD OF PAYMENT (check one)

1. ☐ The Commissioner is hereby authorized to charge indicated fees and credit any overpayments to:

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## FEE CALCULATION

### 1. BASIC FILING FEE

| Large Entity Fee Code | Large Entity Fee ($) | Small Entity Fee Code | Small Entity Fee ($) | Fee Description | Fee Paid |
|---|---|---|---|---|---|
| 101 | 690 | 201 | 345 | Utility filing fee | 710.00 |
| 106 | 310 | 206 | 155 | Design filing fee | |
| 107 | 480 | 207 | 240 | Plant filing fee | |
| 108 | 690 | 208 | 345 | Reissue filing fee | |
| 114 | 150 | 214 | 75 | Provisional filing fee | |

SUBTOTAL (1) ($) 710.00

### 2. EXTRA CLAIM FEES

| | Extra Claims | | Fee from below | Fee Paid |
|---|---|---|---|---|
| Total Claims 16 | -20** = 0 | X | 18 | = 0 |
| Independent Claims 6 | - 3** = 3 | X | 80 | = 240 |
| Multiple Dependent | | | | = 0 |

***or number previously paid, if greater; For Reissues, see below*

| Large Entity Fee Code | Large Entity Fee ($) | Small Entity Fee Code | Small Entity Fee ($) | Fee Description |
|---|---|---|---|---|
| 103 | 18 | 203 | 9 | Claims in excess of 20 |
| 102 | 78 | 202 | 39 | Independent claims in excess of 3 |
| 104 | 260 | 204 | 130 | Multiple dependent claim, if not paid |
| 109 | 78 | 209 | 39 | ** Reissue independent claims over original patent |
| 110 | 18 | 210 | 9 | ** Reissue claims in excess of 20 and over original patent |

SUBTOTAL (2) ($) 240.00

## FEE CALCULATION (continued)

### 3. ADDITIONAL FEES

| Large Entity Fee Code | Large Entity Fee ($) | Small Entity Fee Code | Small Entity Fee ($) | Fee Description | Fee Paid |
|---|---|---|---|---|---|
| 105 | 130 | 205 | 65 | Surcharge - late filing fee or oath | 0.00 |
| 127 | 50 | 227 | 25 | Surcharge - late provisional filing fee or cover sheet. | 0.00 |
| 139 | 130 | 139 | 130 | Non-English specification | 0.00 |
| 147 | 2,520 | 147 | 2,520 | For filing a request for reexamination | 0.00 |
| 112 | 920* | 112 | 920* | Requesting publication of SIR prior to Examiner action | 0.00 |
| 113 | 1,840* | 113 | 1,840* | Requesting publication of SIR after Examiner action | 0.00 |
| 115 | 110 | 215 | 55 | Extension for reply within first month | 0.00 |
| 116 | 380 | 216 | 190 | Extension for reply within second month | 0.00 |
| 117 | 870 | 217 | 435 | Extension for reply within third month | 0.00 |
| 118 | 1,360 | 218 | 680 | Extension for reply within fourth month | 0.00 |
| 128 | 1,850 | 228 | 925 | Extension for reply within fifth month | 0.00 |
| 119 | 300 | 219 | 150 | Notice of Appeal | 0.00 |
| 120 | 300 | 220 | 150 | Filing a brief in support of an appeal | 0.00 |
| 121 | 260 | 221 | 130 | Request for oral hearing | 0.00 |
| 138 | 1,510 | 138 | 1,510 | Petition to institute a public use proceeding | 0.00 |
| 140 | 110 | 240 | 55 | Petition to revive - unavoidable | 0.00 |
| 141 | 1,210 | 241 | 605 | Petition to revive - unintentional | 0.00 |
| 142 | 1,210 | 242 | 605 | Utility issue fee (or reissue) | 0.00 |
| 143 | 430 | 243 | 215 | Design issue fee | 0.00 |
| 144 | 580 | 244 | 290 | Plant issue fee | 0.00 |
| 122 | 130 | 122 | 130 | Petitions to the Commissioner | 0.00 |
| 123 | 50 | 123 | 50 | Petitions related to provisional applications | 0.00 |
| 126 | 240 | 126 | 240 | Submission of Information Disclosure Stmt | 0.00 |
| 581 | 40 | 581 | 40 | Recording each patent assignment per property (times number of properties) | 40.00 |
| 146 | 690 | 246 | 345 | Filing a submission after final rejection (37 CFR § 1.129(a)) | 0.00 |
| 149 | 690 | 249 | 345 | For each additional invention to be examined (37 CFR § 1.129(b)) | 0.00 |
| Other fee (specify) | | | | | 0.00 |
| Other fee (specify) | | | | | 0.00 |

* Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 40.00

## SUBMITTED BY

Complete *(if applicable)*

| | | | | | |
|---|---|---|---|---|---|
| Name (Print/Type) | Carl I. Brundidge | Registration No (Attorney/Agent) | 29,621 | Telephone | 703-312-6600 |
| Signature | | | | Date | 11-27-00 |

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367.393268X00

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicants: S. NORSKOV

Serial No.: Not yet assigned

Filed: November 27, 2000

For: GROUND PLANE FOR A SEMICONDUCTOR CHIP

Group: Not yet assigned

Examiner: Not yet assigned

**PRELIMINARY AMENDMENT**

Assistant Commissioner for Patents
Washington, D.C. 20231

November 27, 2000

Sir:

Prior to examination, please amend the above-identified application as follows.

**IN THE SPECIFICATION**

Please amend the specification as follows:

Page 8, line 15, delete "What is claimed is:".

**IN THE CLAIMS**

Page 9, line 1, insert --What is claimed is:--

Please cancel claims 14-16 without prejudice or disclaimer of the matter therein.

Please amend claims 3 and 5-10 as follows:

3. (Amended) Ground plane according to claim 1 [or 2], wherein the dielectric layer is an integral part of said chip.

5. (Amended) Ground plane according to claim 3 [or 4], wherein said dielectric layer comprises silicon oxide.

6. (Amended) Ground plane according to [one of the proceeding claims] claim 1, wherein said second capacitor plate comprises a layer of conductive glue.

7. (Amended) Ground plane according to [any of the preceding claims] claim 1, wherein said capacitor plate is a metallic layer on said supporting member.

8. (Amended) Ground plane according to claim [claims] 6 [and 7], wherein said layer of conductive glue is provided between said metallic layer and said dielectric layer.

9. (Amended) Ground plane according to [one of the proceeding claims] claim 1, wherein said at least one electrically conducting via extending through said supporting member is directly connected to the second capacitor plate.

10. (Amended) Ground plane according to claim 7[,8 or 9], wherein said vias and said metallic layer are integrally formed from the same metal.

Please add new claims 17-21 as follows:

-- 17. Ground plane according to claim 2, wherein the dielectric layer is an integral part of said chip.

18. Ground plane according to claim 4, wherein said dielectric layer comprises silicon oxide.

19. Ground plane according to claim 7, wherein said layer of conductive glue is provided between said metallic layer and said dielectric layer.

20. Ground plane according to claim 8, wherein said vias and said metallic layer are integrally formed from the same metal.

21. Ground plane according to claim 9, wherein said vias and said metallic layer are integrally formed from the same metal.--

**IN THE ABSTRACT**

Line 12, delete "Fig. 1".

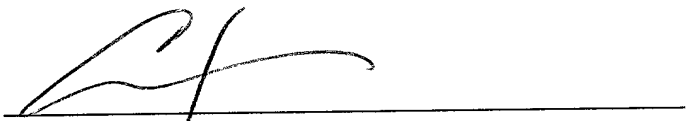
## REMARKS

Entry of the above amendments prior to examination is respectfully requested.

Please charge any shortage in fees due in connection with the filing of this paper, or credit any overpayment of fees, to the deposit account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (367.39268X00).

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP



Carl I. Brundidge
Registration No. 29,621

CIB/jdc
(703) 312-6600

# Ground plane for a semiconductor chip.

## Background of the invention

The present invention relates to the design and production of integrated circuits and to the packaging of such circuits, more specifically the proposed invention relates to a ground plane for a semiconductor chip adapted to be mounted on a supporting member in a chip package.

In all analogue circuit design it is desirable to have a ground that is as close to 0 volt AC as possible. Normally circuit design assumes that ground nodes do not carry any AC-voltage. If a ground node, contrary to this assumption, does carry an AC-voltage, this may lead to unpredictable behaviour, e.g. increased noise, distortion or even instability. The root cause of this is that all conductors have a non-zero impedance. This means that when a ground node has to source or sink a current there will be a voltage drop between it and the actual ground point. This effect is much more pronounced in RF-circuits because the inductive nature of the impedance.

In integrated circuits the ground point of the die (semiconductor chip) is connected to the exterior via a bonding wire connected between the die and the interposer (or leadframe). The impedance of the bonding wire is important at RF-frequencies, and this makes it difficult to realise a proper ground node on the die. If the die is made bigger in order to make the bonding wire shorter, this only moves the problem from the bonding wire to the die because the conductor on the die has to be longer.

Several solutions has been proposed to solve this problem. One is to make the IC-package very small and the bonding wires short. This solution has several

drawbacks. It is only viable for small scale integration circuits. In large scale integration circuits the die is larger and the ground conductors on the die are correspondingly longer. And even for small scale integrated circuits it only reduces the problem, but does not solve it.

Another solution is to have multiple conductors in parallel. This is often used in RF-PA-stages, but is not really practical for large scale integrated circuits as the multiple connections take up a lot of space

Summary of the invention

According to a first aspect of the invention an AC-ground plane is provided for a semiconductor chip adapted to be mounted on a supporting member in a chip package, wherein said ground plane comprises at least one first capacitor plate provided within said chip, and at least one second capacitor plate provided on said supporting member, said first and second capacitor plate being separated by a dielectric layer and capacitively coupled to each other via this layer, and said ground plane comprising at least one first conducting member, said first conducting member being at least one electrically conducting via extending through said supporting member and electrically coupled in series with said second capacitor plate.

According to a second aspect of the invention an AC-ground plane is provided for a semiconductor chip adapted to be mounted on a supporting member in a chip package, comprising a capacitor and an inductor having a resonant frequency which approximately equals the working frequency of the integrated circuit.

According to a third aspect of the invention there is provided a method for providing a tuned RF-ground plane for a semiconductor chip mounted on a supporting member in a chip package. The method includes steps of providing

a metal covered area on the surface of said supporting member, and providing a number of vias electrically connected to said metal covered area and extending therefrom through said supporting to the opposite side thereof, connecting in parallel at least two of said number of vias.

In general terms according to the present invention the problem is solved by placing a metal-covered area on the interposer under the die. Vias on the interposer connect the area to the underside of the interposer. The die is glued to the area with conducting glue. A capacitor is thus formed, the capacitor being formed by the die substrate, the oxide layer on the underside of the die, and the conductive plate on the interposer. By making all other associated impedances as small as possible, e.g. by connecting the metal-plate on the top side of the interposer to the bottom side by using multiple vias in parallel, the resulting impedance can be made very low, less than 20 Ohms, even at high frequencies. If the integrated circuit has a well defined working frequency, the RF-ground plane can be tuned to that frequency by choosing the dimensions of the associated conductors, and the thus the inductance of said conductors, so that the resonant frequency of said inductance and capacitor coincides with said working frequency. The impedance at said working frequency can be made extremely low, close to 2 Ohm.

According to a third aspect of the invention there is provided a semiconductor chip package comprising a semiconductor chip and a supporting member, said supporting member comprising at least one metal covered area and at least one electrically conductive via extending from said metal covered area through said supporting member. The semiconductor chip package is characterised in that the chip is adhered to the supporting member by means of conductive glue and that said conductive glue is in electrical contact with said metal covered area.

The invention will now be described in more detail, by means of the drawings, which show non-limiting exemplary embodiments of the invention.

## Brief Description of the Drawings

Fig. 1 schematically shows a cross section of the preferred embodiment of a semiconductor chip and interposer assembly of an integrated circuit package according to the invention in a situation where the assembly is mounted on a printed circuit board (PCB).

Fig. 2 shows a top plan view of the chip and interposer assembly of fig. 1.

Fig. 3 schematically shows an electric circuit diagram for the LC series circuit of the chip and interposer assembly of fig. 1.

Fig. 4 schematically shows impedance characteristics for the bonding wire and via, and the total impedance, respectively, for the preferred embodiment.

## Detailed Description of the invention

Referring first to fig 1, there is shown a semiconductor chip 1. The semiconductor chip includes an insulating layer 2. Typically this layer 2 would be an integrally formed layer comprising an oxide of the semiconductor material, i.e. silicon dioxide if the chip is made from silicon. The dielectric coefficient of silicon dioxide is app. 3.9.

The chip 1 is glued to an insulating interposer 4 carrying a conductive area 5. Typically the conductive area 5 is a metal covered area. The glue 3 is conductive and serves not only the purpose of adhering the chip 1 to the interposer 4, but also forms a capacitor plate, capacitively coupled to internal parts (not shown) of the chip, but insulated therefrom by the insulating layer 2.

In the following these internal parts are referred to as capacitor plates regardless of their actual shape, i.e. all current carrying parts within the chip are considered as forming capacitor plates.

From the conductive area 5 on the surface of the interposer 4 a number of vias 7 extend through the interposer 4 to the opposite surface thereof, where they may be contacted by a printed circuit board (PCB) 10.

In this respect it should be noticed that even though the metal coated area in the embodiments shown corresponds largely to the dimensions of the chip this is not a prerequisite for the invention to work. Instead, because the conductive glue defines the capacitor plate vis-à-vis the internal parts, it is in principle sufficient to contact the glue 3 to the vias 7.

Even though it could be imagined that the metal covered area 5 on the interposer 4 could provide the capacitor plate directly, i.e. instead of providing the capacitor plate in by means of conductive glue 3, this is less desirable.

There are several reasons for this. Using a non-conductive glue between the chip 1 and the metal covered area 5, increases the thickness of the dielectric insulating material between the capacitor plates and thus decreases the capacitance value for the capacitor $C_5$ thus formed. Further the thickness of the glue will be much less well defined than the thickness of the insulating layer 2, such as a silicon dioxide layer, on the chip, which, due to the precision in the manufacturing process for the chip 1, may be made very thin and well defined.

The capacitance value has been found to be approximately ten times higher when using conductive glue as compared to non-conductive glue.

Thus without the conductive glue 3 the capacitance value becomes both smaller and less predictable.

The vias 7 form a conducting member which connects the second capacitor plate to an exterior ground node according to the invention.

Though each via 7 at the frequencies of interest only exhibits a relatively small impedance, it will in the envisaged applications be important to have a large number of vias 7 coupled in parallel in order to lower the impedance further over a range of frequencies.

Thus, in order to have as many vias 7 as possible and the best possible electrical connection from the glue to these it is desirable to have a large metal covered area, preferably formed integrally with the vias 7.

It is known that any conducting member exhibit an inductance. Thus, an LC series circuit is formed by the capacitance provided between internal parts of the chip and the conductive glue 3 separated by the dielectric layer 2, and the inductance provided by the vias 7. If the chip has a well defined working frequency, the number of vias may be chosen, so that the series resonant frequency of the inductance provided by the vias and the aforementioned capacitance, approximately matches the working frequency of the chip. In this way an extremely low ground impedance, 2 Ohms or less, can be achieved.

It should be noted that the vias 7 in the preferred embodiment are not connected in parallel directly on the supporting interposer 4. Instead they are, as shown in fig. 5, connected in parallel via the conductive paths 16 on the printed circuit board 10 on which the chip package, containing the chip 1 and interposer 4 assembly according to the invention, is eventually mounted.

This is only to illustrate one way of connecting the vias 7 in parallel, and numerous other ways may be devised by the skilled person.

In particular it should be noted, that the resonant frequency of the ground plane is influenced by the number of vias 7 actually connected in parallel for a given application, and by the way this is done, as well as by the inductance of the die and the layout of the PCB 10.

Further, as shown in fig. 1, a number of DC ground paths may be provided.

A ground pad 13 is connected to a via 6 through a bonding wire 8 which in turn is connected to the PCB ground plane 12 by via 14. The impedance of this path is essentially inductive at the frequencies of interest.

Another ground pad 15 is connected to conducting member 11 on interposer 4 through bonding wire 9 which is connected to the PCB ground plane 12 by vias 7. Either, or both, of the above described DC ground paths may be used. It should be noted that most circuits require at least one DC ground path.

The DC ground paths may also be used for AC signals if very low ground impedance is not required.

The components in the diagram carries indices corresponding to the reference numerals on fig. 1. Thus $L_1$ is the inductance of the die itself, $L_8$ is the inductance of the bonding wire 8, $L_{14}$ the inductance of the via 14, $C_5$ the capacitance between internal parts of the chip 1 and the capacitor plate provided by the glue 3, $L_9$ the inductance of bondwire 9, $L_{11}$ the inductance of conducting member 11 on interposer 4, and $L_7$ the combined inductance of the vias 7, when they are eventually connected in parallel.

Fig. 4 illustrates the difference between the impedance to ground when an AC-ground plane according to the invention is used (normal line), and when only the inductive DC ground is used (dotted line). Both axes are logarithmic. In particular the dip in impedance at $f_0$ should be noted, since at this specific frequency the impedance of the ground path becomes virtually zero. Thus if this frequency $f_0$ matches the operating frequency of the chip, a very low impedance ground path is provided for the chip. However, even if $f_0$ is not tuned to the working frequency of the circuit the ground impedance obtained by using the AC-ground plane is still much lower that it would have been without it provided that the working frequency of the circuit is greater than $f_a$

It has been found that using the an AC-ground plane according to the invention there may be provided a substantial noise reduction at desired frequencies.

What is claimed is:

1. A ground plane for a semiconductor chip adapted to be mounted on a supporting member in a chip package, wherein said ground plane comprises at least one first capacitor plate provided within said chip, and at least one second capacitor plate provided on said supporting member, said first and second capacitor plate being separated by a dielectric layer and capacitively coupled to each other via this layer, and said ground plane comprising at least one first conducting member, said first conducting member being at least one electrically conducting via extending through said supporting member and electrically coupled in series with said second capacitor plate.

2. Ground plane according to claim 1, wherein the resonant frequency of the capacitance provided by said first capacitor plate and said second capacitor plate, and the inductance provided by said first conducting member, is approximately equal to the intended working frequency of said chip.

3. Ground plane according to claim 1 or 2, wherein the dielectric layer is an integral part of said chip.

4. Ground plane according to claim 3, wherein said dielectric layer covers the entire surface of the chip facing the supporting member.

5. Ground plane according to claim 3 or 4, wherein said dielectric layer comprises silicon oxide.

6. Ground plane according to one of the proceeding claims, wherein said second capacitor plate comprises a layer of conductive glue.

7. Ground plane according to any of the preceding claims, wherein said capacitor plate is a metallic layer on said supporting member.

8. Ground plane according to claims 6 and 7, wherein said layer of conductive glue is provided between said metallic layer and said dielectric layer.

9. Ground plane according to one of the proceeding claims, wherein said at least one electrically conducting via extending through said supporting member is directly connected to the second capacitor plate.

10. Ground plane according to claim 7, 8 or 9, wherein said vias and said metallic layer are integrally formed from the same metal.

11. Method for providing a ground plane for a semiconductor chip mounted on a supporting member in a chip package, characterised in providing a metal covered area on the surface of said supporting member, providing a number of vias electrically connected to said metal covered area and extending therefrom through said supporting to the opposite side thereof, connecting in parallel at least two of said number of vias.

12. Method for providing a tuned ground plane for a semiconductor chip mounted on a supporting member in a chip package according to claim 10, wherein the semiconductor chip is adhered to said supporting member by means of a conductive glue.

13. Semiconductor chip package comprising a semiconductor chip and a supporting member, said supporting member comprising at least one metal covered area and at least one electrically conductive via extending from said metal covered area through said supporting member, wherein said chip is adhered to the supporting member by means of conductive glue and that said conductive glue is in electrical contact with said metal covered area.

14. LC series circuit for a semiconductor chip substantially as herein before described with reference to figs. 1-4 of the accompanying drawings.

15. Method for providing a tuned RF-ground plane for a semiconductor chip mounted on a supporting member in a chip package substantially as herein before described with reference to figs. 9-10 of the accompanying drawings.

16. Semiconductor chip package comprising a semiconductor chip and a supporting member substantially as herein before described with reference to figs. 1-4 of the accompanying drawings.

## ABSTRACT

AC-ground plane is for a semiconductor chip adapted to be mounted on a supporting member in a chip package, wherein said ground plane comprises at least one first capacitor plate provided within said chip, and at least one second capacitor plate provided on said supporting member, said first and second capacitor plate being separated by a dielectric layer and capacitively coupled to each other via this layer, and said ground plane comprising at least one first conducting member, said first conducting member being at least one electrically conducting via extending through said supporting member and electrically coupled in series with said second capacitor plate.

Fig. 1

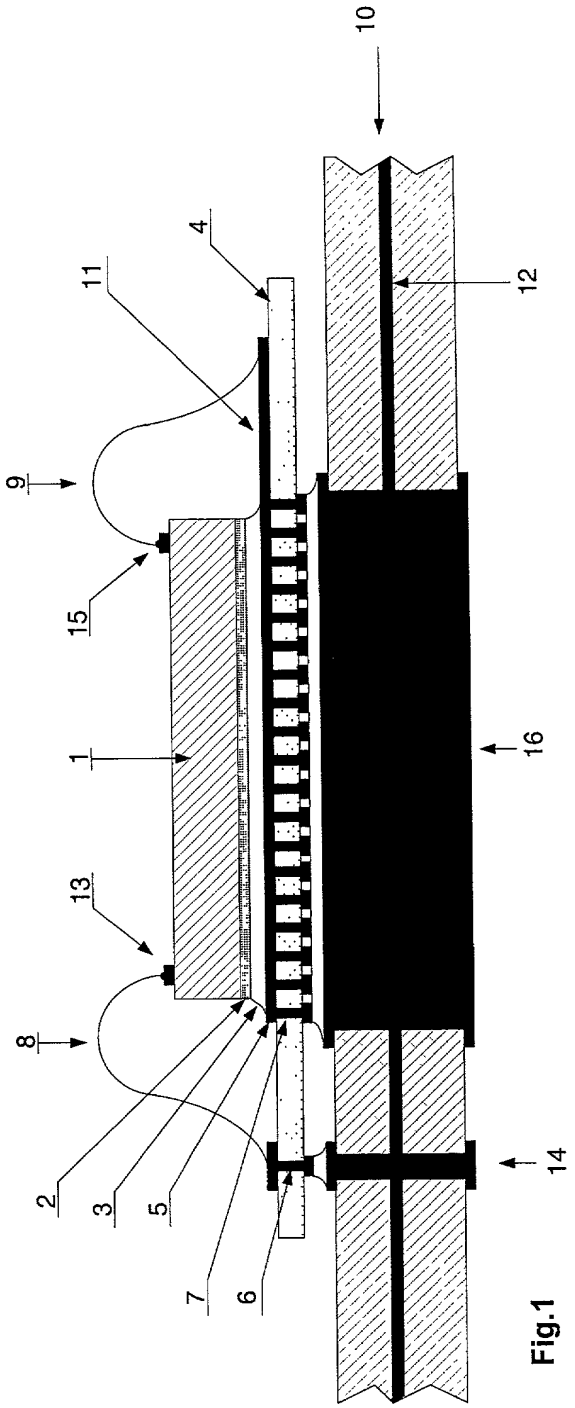



Fig.1

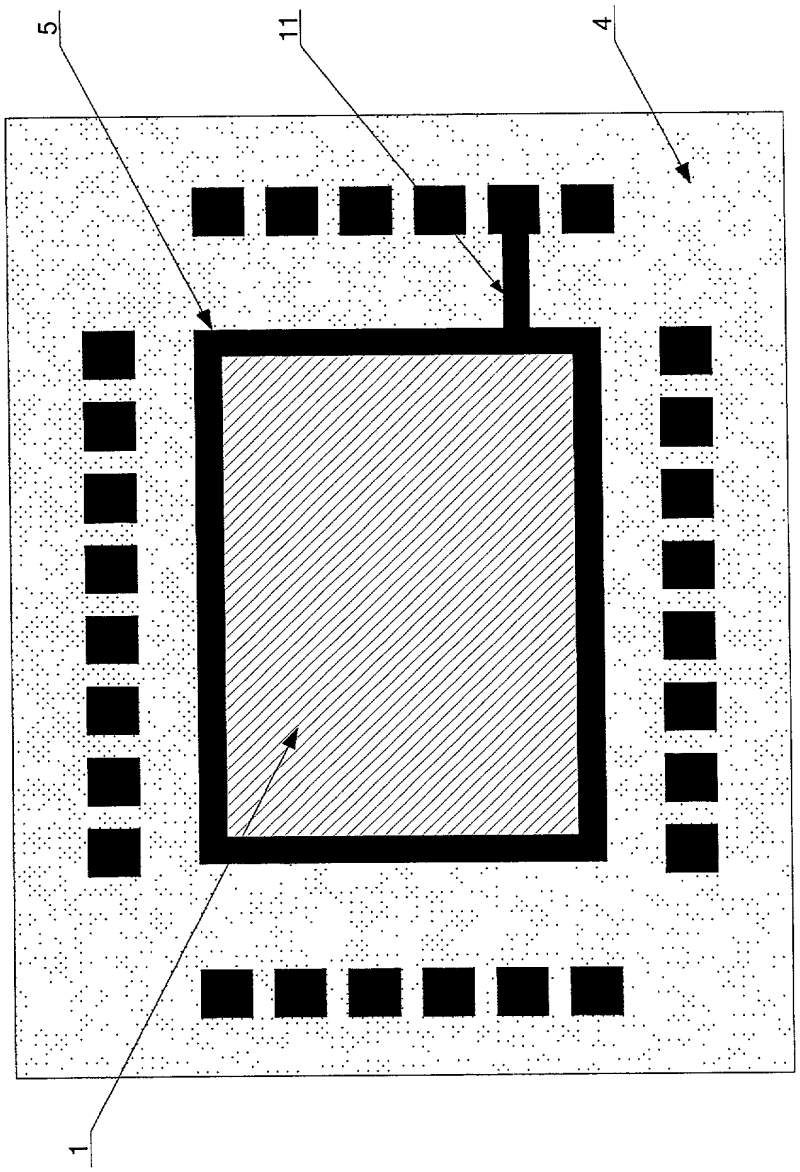



Fig.2

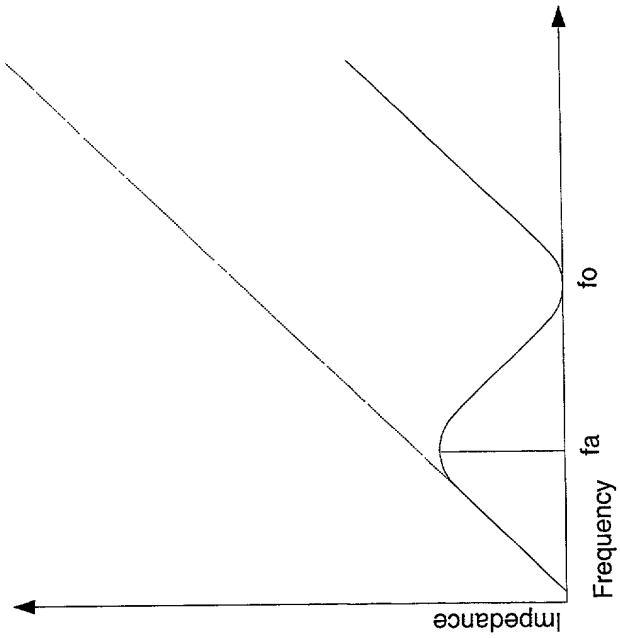



Fig. 4

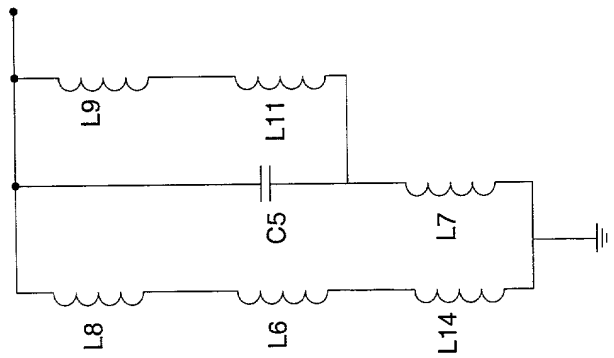



Fig. 3

## DECLARATION AND POWER OF ATTORNEY - PATENT APPLICATION

As a below named inventor, I hereby declare: that my citizenship, residence and post office address are as stated below; that I verily believe I am the original, first and sole inventor (if only one is named below) or a joint inventor (if plural inventors are named below) of the invention entitled:

**Ground plane for a semiconductor chip**

the specification of which __X__ is attached hereto

__ was filed on _____ as Application Serial No. _____ and was amended on _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a). I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

| Prior Foreign Application(s) | | | Priority Claimed |
|---|---|---|---|
| GB 9928080.2 | GB | 26/11/1999 | YES |
| Number | Country | Day/Month/Year Filed | Yes /~~No~~ |

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application;

| Application Serial No | Status-patented, pending or abandoned |
|---|---|

I hereby appoint as principal attorneys: Donald R. Antonelli, Reg. No. 20,296; David T. Terry, Reg. No. 20,178; Melvin Kraus, Reg. No. 22,466; William I. Solomon, Reg. No. 28,565; Gregory E. Montone, Reg. No. 28,141; Ronald J. Shore, Reg. No. 28,577; Donald E. Stout, Reg. No. 26,422; Alan E. Schiavelli, Reg. No. 32,087; James N. Dresser, Reg. No. 22,973, Carl I. Brundidge, Reg. No. 29,621; and Paul J. Skwierawski, Reg. No. 32,173; to prosecute and transact all business in the Patent and Trademark Office connected with this application and any related United States and international applications.

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

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